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Partial Dynamic Reconfiguration For Enhancing Fault Tolerance In System-On-Chip Designs

[#1]B.SAIRAM, *M.Tech(DSCE) Student,*
[#2]B. SANTHOSH, Associate Professor & HOD,
Department of ECE,
MOTHER THERESSA COLLEGE OF ENGGINEERING, PEDDAPALLI,TG

ABSTRACT: This research demonstrates a novel approach to enabling intrinsic repair by modifying the settings of Software Defined Radio (SDR) devices that are constructed on Field-Programmable Gate Arrays (FPGAs). The primary objective is to develop a real-time adaptive system that can rapidly adapt and manage errors in order to satisfy mission-critical requirements. The research indicates that the utilization of a Virtex 6E FPGA to construct the system results in a 40% reduction in energy consumption when reliability levels decrease to 0.75. In high-reliability systems with a reliability coefficient above 0.90, it only saves 30% of the energy; however, triple modular redundancy still effectively safeguards against faults. Performance-Driven Regulation (PDR) is an effective method for enhancing system performance. After implementation, it raises efficiency by 32.61 percent and output by 14.61 percent.

Keywords: *Software Defined Radio; Partial Dynamic Reconfiguration; Fault Tolerant; Low Power; Reliability; SignalProcessing; FPGA.*

1. INTRODUCTION

Software Defined Radios (SDRs) play a crucial role in many space-related disciplines, including meteorology, geographical information systems, and navigation. Because they are software-based, they can change their behavior while in orbit. Because SDRs built on Field-Programmable Gate Arrays (FPGAs) can handle a lot of processing and can be changed to accommodate new protocols on the fly, this is very important for space missions. But FPGAs can only do what the configuration data they store in memory can do. They have SRAM configuration memory, which makes reconfiguring them easy, but they are also vulnerable to SEUs. These mistakes pose a significant threat because they can cause systems to become unusable. Conditions in space or where numerous designs are implemented on a single FPGA increase the risk. Because of this, attempts to reduce SEU are necessary but not sufficient.

To guarantee their functionality, modern real-time systems often use programmable hardware or application-specific integrated circuits (ASICs). Due to their complexity, these systems, especially when configured as system-on-a-chip (SOC) devices, place a premium on reliability and fault tolerance (FT). Because of the dire repercussions that could result from data loss or delays, mission-critical systems must always function correctly. The reduced voltage and current thresholds, along with process modifications like sub-wavelength lithography or random dopant

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fluctuations, make design errors more common in sub-micron SOC systems. Repairing and maintaining these systems is an expensive and time-consuming ordeal, so it's important to have strong FT designs with testability (DFT) to deal with frequent failures.

With the increasing complexity and interconnection of systems, FT systems must adapt to handle and resolve issues autonomously in real time. Improved FT system reliability and efficiency should be a byproduct of signal processing systems' ability to provide change-responsive, real-time corrections. An essential part of FT designs is redundancy, which involves having backup parts that can still work if the main parts fail. Having many of something makes it more reliable, but it's more costly, uses more energy, and takes more time to design, test, and verify. For FT systems to keep being useful and adaptable, they need to figure out how to fix these problems.

A better long-term solution to these issues is Partial Dynamic Reconfiguration (PDR). Triple Modular Redundancy (TMR) and split systems are the two most common conventional approaches to hardware backup. Despite the redundancy levels offered by simple, duplex, and TMR, modern methodologies place a premium on speed and stability. While there are some cases where TMR is still the best option, there are also cases where just one setup will do. By considering dimensions, power consumption, critical path latency, and different signal processing circuits, this research finds the most fault-tolerant designs for SDR systems. It also brings a new way for FPGA-based SDR systems to handle errors, making it easier to find and fix problems. This cutting-edge innovation improves SDR systems' dependability and performance by automatically adjusting to the needs of real-time applications.

2. FAULT HANDLING RECONFIGURATION ALGORITHM - CONTROL FLOW OF DETECTION AND REPAIR PROCESS

The suggested defect management control system aims to lessen the frequency of system failures and increase the system's reliability. Fixing stuck-at-0/1 errors requires a new approach to fault management. With this algorithm, we can shorten the MTTR and lengthen the MTBE, or Mean Time Between Errors. Using fault-tolerant (FT) strategies, the system ensures its availability and efficiency. In order to detect and fix problems in real time while keeping them hidden during repairs, this method uses a TMR or duplex plan with online checkers, as shown in Figure 1. As a result, the system for preventing failure is very strong.

Module Error Correction

The system will automatically switch to duplex mode to start the module recovery process if a simplex mode malfunction occurs. Using the duplex mode web tester, the equipment can be put back together in the same way it was before the module failed. It is highly likely that Single Event Upsets (SEUs) are the cause of any issues that continue. These problems can be fixed by using setup bit files that are specific to each module. During the repair process, the problematic components are removed from the module that is not working

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properly. Sending an error signal to the partial reconfiguration controller (PRC) starts the recovery process if the online checker detects issues in two-way mode.

The PRC then uses a two-step healing process to resolve the error by loading the bit files required by the broken module. This method is better than editing each file by hand because it fixes issues faster. To recover bits that have been lost after a device reset, this method solely uses the Packet Delivery Ratio (PDR). Importantly, watchdog timers detect problems that continue after hardware repairs and send command signals to start the second stage of recovery.

When it comes to the Mean Time To Repair (MTTR), both recovery phases can get non-functioning modules up and running again. When two units fail at the same time and the MTTR is greater than the MTBE, the system may not work properly. If these methods of deterministic recovery do not work, the system will switch to Triple Modular Redundancy (TMR) mode. At this point, we fix the broken modules using a recovery method based on Genetic Algorithms (GA), which uses cutting-edge techniques to get the system working again.

Due to the repetitive nature of the recovery process required to resolve issues, the mean time to detect (MTTD) is reduced to zero when a TMR defect occurs. To make sure that TMR errors are handled quickly and don't cause any more problems, they are addressed at regular intervals. Nevertheless, fixing errors that keep happening even after trying everything else is a tough nut to crack, and reliable systems need advanced recovery mechanisms.

System Framework for the Proposed Fault Handling Algorithm

After testing with the system's PRFR and static reconfiguration controller region (SRCR), the problem-solving strategy was found to be successful. The SRCR's control software and PRC are its two main parts. Notify the PRC immediately if a PRM faces any problems. Fault recovery must begin while the software is running, so having a reliable tool that can detect errors instantly is crucial. It should be possible, if possible, to install circuits that allow people to independently detect problems, even if they need supplementary tools. The analyzer will send out an error signal if it finds a problem with a function unit. The output from the function unit is checked by the validator to ensure accuracy.

Figure 1: Make a rundown of all the steps that the system's fault management system will take.

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3. Implementation Steps and Results of the Partial Dynamic Reconfiguration

Xilinx programming tools, you can choose between FPGAs and SOCs. A sixteen-part ISE series The PDR is provided with a consistent approach to task management by Xilinx Plan Ahead. Every single step has to be carried out exactly as planned for the whole process to work. Public register messages (PRMs), sometimes called bus macros, allow maintenance-required modules to communicate with the rest of the system ("static logic").

Elements can share information and data via these connections. In order to create the partially customizable netlist, we followed the synthesis criteria. Following public relations design guidelines, the floor plan's static devices are placed near the PRMs. It is necessary to compare the partial reconfiguration design to the PDR design rule tests before the settings are activated and bit files are generated.

By using a black box section, bitgen can create a blanking bit file. An element known as a "black box" is now part of the self-healing system. We compare FFT_2 with FFT_1. A specific AREA_GROUP range must be specified for each partition's actual resources. This investigation allows for the modification of FFT_1 and FFT_2. In FFT_1, you'll find the validation and the initial FFT block. FFT_2 includes the second FFT block and the verifier that goes along with it. Data stored in permanent code does not have any restrictions imposed by a moveable split's AREA_GROUP range. Figure 2 depicts the process of assembly.

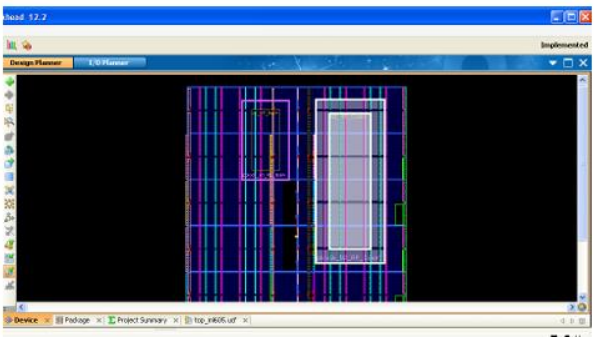

Figure 2: The help of modules FFT_1 and FFT_2, one can change the layout of a room.

We take a look at each circuit in our case research and see how much space and energy it could save with and without PDR. Implementations of duplex2ch and tmr3ch result in a percentage decrease, as shown in Figure 3. On average, PDR systems increase resource use by 32.61%, while electricity use and economy grow by 14.61%.

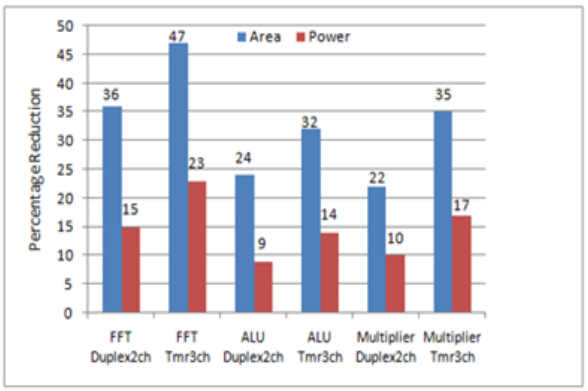

Figure 3: A substance that is used to strengthen and enlarge an object's surface area.

Evaluation of Power Savings due to Adaptive Approach

The best ways to save power over an application's lifetime are to set up a no-fault state and lower the reliability demand. During operation, the PFE indicates the power consumption of one FU and monitor. PV is a measure of an

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individual's typical power usage. A standard TMR's PTMR indicates the power needed to move it. The PADAP is an example of a flexible device that can change its power consumption as needed. The adaptive system has supplanted the old TMR because it uses less energy.

$$P_S = \frac{P_{TMR} - P_{ADAP}}{P_{TMR}}$$

$$P_S = \frac{(2 - R)\, P_{FE}}{3 P_{TMR}}$$

The conditions are met, the adaptive TMR can be used instead of the conventional TMR to conserve power, as shown in Equation (2). In order to find out how much energy the system will save when all three modes are used at once, we use Equation (3).

$$P_S = \frac{R_{PV} + 2 P_{FE}}{3 P_{TMR}}$$

Equations 2 and 3 show that the adaptive system works better when the reliability requirement is average or low. Its ability to run for long durations with minimal power consumption is the reason behind this. By tracking the power usage of each part of the system with the Xilinx X Power analyzer (XPA), we were able to verify that the theoretical findings were supported by practical evidence.

Xilinx power estimators (XPE) are separate from Xilinx ISE design suite and use mapping data instead of placement or route data to estimate a device's power consumption. On the other hand, Xilinx power analysis (XPA) takes into account both kinds of information. Table 1 shows that compared to the TMR, the adaptive FT system uses less power while still maintaining a high degree of reliability. At an R-value of 0.75—corresponding to a 30% mission sustainability rate—the suggested adaptive strategy starts to lower the cost of electricity. There is a statistically significant correlation between the reliability of mission-critical and non-critical systems (R = 0.75).

As low as a R value of 0.75, FlexFT is able to preserve more than 40% of energy. For highly reliable systems (R > 0.90), the benefit drops to 30%, but the fault-protection features of TMR are unaffected. Creating a system that meets medium to high reliability standards while minimizing speed loss was within the realm of possibility. However, more energy was saved by programs whose only purpose was to increase reliability. To the contrary, stability is not crucial to the system's operation for the most part.

Table 1 What Effects XPA Has on Electricity Rates

Reliability	P_s (%)
1 %	60.14
21 %	50.32
50 %	45.22
70 %	40.19
90 %	35.33
97 %	30.33
99 %	29.99
100 %	28.86

4. CONCLUSION

Balanced system design with little speed loss is what the Xilinx Virtex6E FPGA can offer if you need moderate to high reliability. There is a marked decrease in the consistency and effort required for the present task. According to the research, the

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suggested framework would make the FT system more accessible and dependable without changing its functionality. To implement adaptive self-healing, engineers need not make changes to preexisting designs or simply account for the worst-case situation.

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